**Pak-Austria Fachhochschule: Institute of Applied Sciences & Technology, Haripur, Pakistan**

**School of Computing Science**



**DLD LAB**

**Lab # 13**

**Submitted By: Haider Nasir**

**Registration # B24S0308AI088**

**Submitted to: Engr. Raghib**

**Date of submission: 5/1/2025**

**Lab 13:**

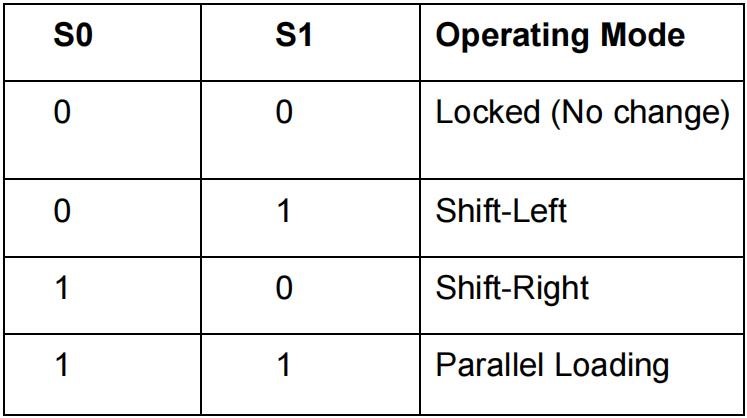
**Design and Implementation of Shift Register on Electronic Workbench (EWB).**

**Section: AI-Blue**

**Objectives:**

To analyze the behavior of shift registers.

To experimentally verify the proper operation of a 4-bit universal shift register.

**Tools/Equipment Requirement:**

PC or Laptop

Electronic Workbench

ICs for D-type flip-flops and 4 x1 multiplexers.

555 Timer

Digital Trainer

**Theoretical Explanation:**

**Shift Register:**

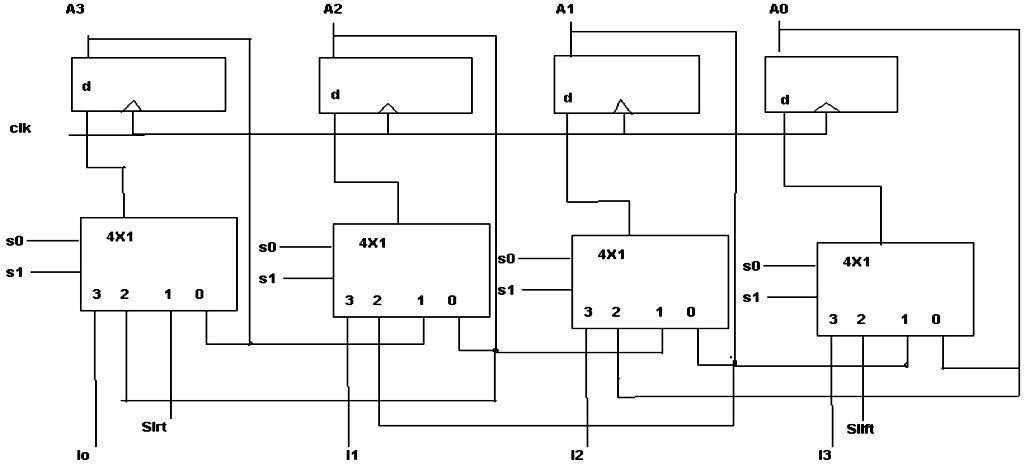
A shift register is a sequential digital circuit that can store and shift binary data. It consists of a series of flip-flops connected in a chain, where the output of one flip-flop becomes the input to the next. Shift registers are used for data storage, data transfer, data manipulation, and in various applications including serial-to-parallel and parallel-to-serial conversion.

A universal shift register, as shown in the circuit/logic diagrams is an integrated logic circuit that can transfer data in different modes. The different modes of operation are as listed in a table below:

The synchronous operation of the device is determined by the mode select inputs (S0, S1). As shown above in the table, data can be entered and shifted from left to right (A0 to A1 to A2, etc.) or, right to left (A3 to A2 to AQ1, etc.) or parallel data can be entered, loading all 4 bits of the register simultaneously. When both S0 and S1 are LOW,existing data is retained in a locked/hold (“do nothing”) mode. The first and last stages provideD-type serial data inputs (Slrt, Sllft) to allow multistage shift right or shift left data transfers without interfering with parallel load operation. The four parallel data inputs (I0 to I3) are D-type inputs. Data appearing on the I0 to I3 inputs, when S0 and S1 are HIGH, is transferred to the A3 to A0 outputs respectively, following the next LOW to-HIGH transition of the clock.

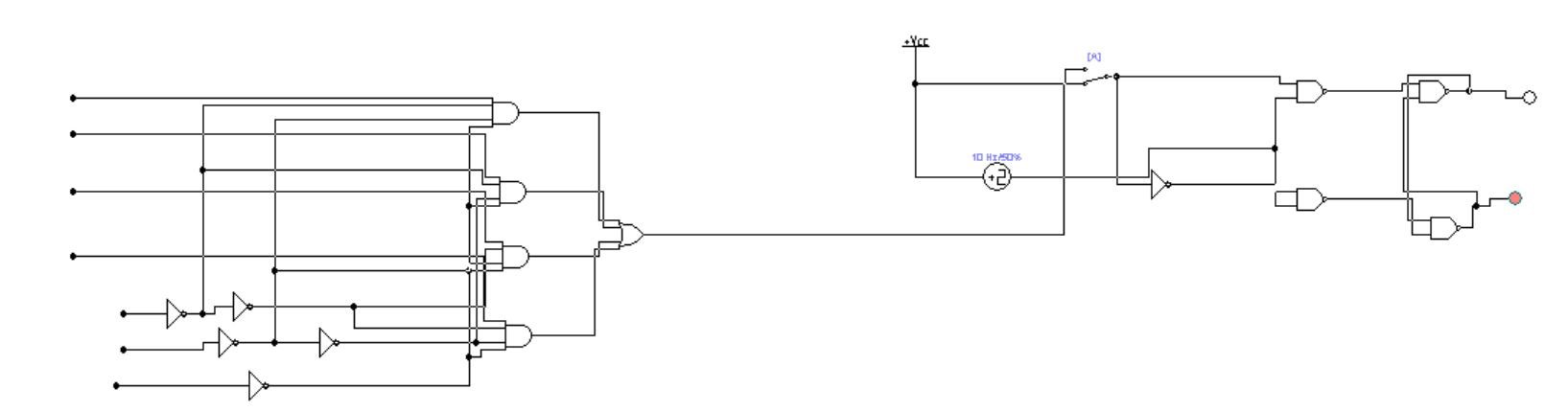
**Procedure:**

1. Implement the circuit of a 4-bit universal shift register as shown below. 2. Verify all modes of operation as discussed above



**Lab Task / Observation:**

**Universal Shift Register:**



**Conclusion:**

In this lab, I successfully implemented a 4-bit universal shift register using Electronic Workbench (EWB). The shift register was tested in various modes, including shifting data left, right, and parallel loading. By controlling the mode select inputs (S0 and S1), We were able to observe the different operations of the register. The circuit functioned as expected, with data shifting correctly and parallel inputs being loaded into the outputs.